A Survey on Network Processors

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Abstract

Network Processors are application specific processors that are used for network domain problems such as packet classification, admission control and intrusion detection. To cope with the changing protocols and high speed network services, communication devices need to be flexible as well as high performing. A Network Processor is a programmable device, consists of some hardware accelerators facilitating flexibility as well as wire speed network operations. In this Paper, we survey on three widely known network processors named PayloadPlus marketed by Agere systems, PowerNP from IBM and IXP1200 from Intel corporation.

Key words: Network processor, PayloadPlus, PowerNP, IXP1200.

1 Introduction

Computer network is used widely for numerous services. The use of computer network is increasing day by day for its simplicity and elegance. Billions of users are connected to computer network now-a-days. High number of users caused bandwidth explosion in past few years. Many new types of services and applications have been introduced in the networking domain. Thus network is demanding technology with higher efficiency and flexibility to support new protocols and applications. Network processor technology is a firm step towards the solution of different networking problems. A network processor is an integrated circuit which has a special set of instructions designed considering networking application domain.

Until recently, functionality of data link layer and above has been performed by software running on generic CPUs. Over the last few years VLSI circuit performance and number of transistors in a die have increased exponentially. So, many hardwired solutions have emerged for higher layer

network protocols. In section 2, we discuss some terms that will be needed to understand the rest of the paper. In section 3, we discuss three network processor architecture and then give a comparison among them. Finally, section 4 concludes with some questions that must be answered for network processors to be easily applicable.

2 Preliminaries

Since network processors are application specific processors, we must have a clear understanding of networking application domains. we refer readers to [6] for more on networking applications. OSI stack model is widely used layering standard for dividing any networking solution into different layers. OSI specifies seven layers. Among the layers, layer 2 which is called *Data Link Layer* (DLL) is responsible for providing reliable communication between two computers using point-to-point link. Layer 3 which is called *Network Layer* (NL) enables communication between two distant computers using the point-to-point links provided by DLL. Network processors primarily attack the functionality of these two layers to provide faster functionality as well as supporting flexibility. The upper layer *i.e.* layer 4-7 functionality can also be performed by network processor.

Network processors employ various techniques to support wire speed performance. One of the widely used technique is parallelism. Parallelism is used in all network processor to enhance speed of execution. A *Processing Element* (PE) is an instruction set processor that decodes its own instruction stream [7]. Each network processor employs multiple PEs either symmetrically or in pipelined fashion to increase parallelism.

3 Network Processors

In this section, we discuss about three network processors. They are PayloadPlus from Agere systems, PowerNP from IBM and IXP1200 from Intel corporation. While studying these network processors, we have outlined mainly the architecture, programmability, interfaces, data rate and performance benefits of them.

3.1 PayloadPlus

PayloadPlus is in the market since the end of 2001. This three chip network processor can perform all sort of classification, quality-of-service, traffic management and shaping, packet modification

etc [1]. The three main parts of PayloadPlus network processor are Fast Pattern Processor (FPP), Routing Switch Processor (RSP) and Agere System Interface (ASI). FPP is a programmable, highly pipelined and multithreaded chip. FPP can accept 64 packets and process them simultaneously. FPP contains a Pattern Processing Engine (PPE) which can perform pattern matching at consistent speed independent of the number of patterns. FPP also contains a CRC engine to recalculate the CRC of incoming packets. It has also some bus interfaces to communicate with other parts and outside world. RSP accepts packets from FPP and process them at wire speed. It has a 64K programmable queue. RSP is mainly responsible for traffic shaping, traffic management and other QoS related operations. ASI is actually a PCI interface between outside devices and PayloadPlus. The interface is used generally for controlling such as routing/virtual circuit table update. ASI also assists in exception handling and hardware configuration. For more on PayloadPlus network processor architecture see [3].

High level application oriented language is used for programming FPP. The functional scripting language, FPL is used to mention the protocol processing in high level format. Similar functional scripting language is used to programme RSP also. PayloadPlus supports 32-bit UTOPIA Level 3/UTOPIA Level 2/POS-PHY Level 3 interface. PayloadPlus is intended to support layer 2-4 processing and can support data rate up to 2.5Gbps.

3.2 PowerNP

PowerNP[1] is a multi-protocol interface supporting networking solution. It can provide wide range of solutions from stand alone system to large network switching fabric. A set of 16 programmable processing engine is present named as *Embedded Processor Complex* (EPC). Each of the processing engine is called *Picoprocessor*. Picoprocessors are grouped into sets of two, known as *Dyadic Protocol Processor Units* (DPPUs). A dispatch unit is responsible for sending the incoming packets to idle Picoprocessors. A Tree Search Engine (TSE) is used to perform table look up in PowerNP. A completion unit is present as interface between processing units and outside world. It also ensures packet sequences which are processed by different processing units. More on PowerNP architecture can be found in [4].

A parallel "run-to-completion" programming model is available to program PowerNP. It presents a single image of packet processing from arrival to departure.Picoprocessors are used as a pool of

[1]In this paper PwerNP is used as the abbreviated form of IBM PowerNP NP4GS3.

processing elements working or idle waiting for packets [1]. PowerNP is intended to facilitate layer 2-5 processing and supports packet over SONET (POS) and Gigabit Ethernet at data rate 2.5Gbps [2].

3.3 IXP1200

Intel IXP1200 is one of the oldest processor in the networking domain. It encompass six micro-engines and a StrongARM. All packet processing tasks are performed by micro engines each supporting four threads. Some special hardware like programmable hash engine and specialized queue facilitates packet processing. StrongARM is responsible for system activity coordination. StrongARM shares the hash engine and specialized queue with micro-engines. 8KB data cache and 16KB instruction cache is present in IXP1200. Moreover a 4KB scratchpad SRAM is also present. More on IXP1200 can be found in [5].

IXP1200 is programmed using macro-assembly. Intel also supplied a C compiler for programming IXP1200. The IDE provides good aid in programming as well as debugging. Intel IXP1200 is intended to support layer 2-4 support. Additional layers can be supported by connecting external processors through PCI interface. IXP1200 can support a packet rate of 2.5Mpacktes/s.

3.4 Comparison

In this subsection, we give a comparative discussion among the network processors we have discussed so far. The aspects that can be used to compare network processors are hardware architecture, parallelism, interfaces, software support etc.

All the network processors are equipped with special hardware to process the packets at wire speed. All of them are intended to support some networking layer functionality. Every network processor exhibits parallelism both in hardware and in software. Despite being intended for networking domain, network processors exhibits various dissimilarity. To summarize the hardware architecture dissimilarity, PayloadPlus and PowerNP both operates on 133MHz clock [3, 4]. IXP1200 can operate at higher 200MHz clock [5]. PowerNP generally consumes more power than other two while IXP1200 consumes the least. PayloadPlus has three main component FPP, RSP and ASI responsible for different functionality. PowerNP has 16 EPC/picoprocessors for main processing and coprocessor for tree searching while IXP1200 has six micro-engines for main processing and special hash engine for extra functionality. In PayloadPlus FPP does the main processing job

which supports 64 different hardware contexts, in PowerNP EPC is responsible for packet processing which supports 2 different hardware contexts and IXP1200 has 4 hardware contexts in each micro-engines. Another important characteristics that can be used is the number of software contexts of a network processor. The software context denotes how many different program can run physically at the same time. A network processor will have as many program counter (PC) as it has software context. It can be noted that, PayloadPlus has three main components, PowerNP has 16 picoprocessors and IXP1200 has 6 micro-engines. So, the number of software contexts in PayloadPlus, PowerNP and IXP1200 are 3, 16 and 6, respectively.

Each processor needs control unit. ASI handles control functions in PayloadPlus, PowerPC and StrongARM provides the same functionality in PowerNP and IXP1200, respectively. Special bus interface is present in payloadPlus to be used in communication between ASI and other components. Dispatch and completion unit handles communication among PEs in PowerNP. IXP1200 also has some fast bus interfaces for communication. External memory is needed to connect with PayloadPlus while PowerNP and IXP1200 has on chip memory. Size of built in memory in PowerNP is 32KB per PE and in IXP1200 it is 4KB shared by all PEs.

All processors are programmable as they must be. Special scripting languages are present to program PayloadPlus. Compiler is available for the scripting languages. Application code interface (ACI) is also available for facilitating programming PayloadPlus. On the other hand, assemblers are available to program PowerNP. IXP1200 supports most programmability which can be programmed in macro-assembly. Assembler is available for that. Moreover, IXP1200 can be programmed in C, compiler suite is provided by Intel team.

4 Conclusion

In this paper, we surveyed three different network processors. We discussed about there architecture and compared them in various aspects like hardware architecture, interfaces and programmability. The analysis of this paper has driven to some critical questions like,

- What is the number of PEs that will enable optimum performance of a network processor?
- Is it possible to design a network processor that can support all protocol suite at optimum speed?
- Can a general programming model can developed to program network processors?

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